ABSTRACT OF THE DISCLOSURE

A memory includes: a memory array having a plurality of storage elements; a plurality of replacement storage elements; a plurality of address fuse units, each having a plurality of fusible links and being operable to store a replacement address, each replacement address identifying one of the storage elements of the memory array to be replaced by an associated one of the replacement storage elements and forming a respective 2^m bit row or 2^n bit column of a fuse array; a vector generator operable to produce a 2^n bit row vector based on the rows of the fuse array and to produce a 2^m bit column vector based on the columns of the fuse array; and a compression unit operable to produce a row checksum from the row vector and to produce a column checksum from the column vector.

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